PRACTICE SET

End Semester Examination, December- 2025

Program: MCA **Course: Computer Organization and Architecture**
Course Code: 3CIT103 **Semester: I**

Course Outcome:

After the successful completion of the course, the students will be able to:

1. Explain the basics of organizational and architectural issues of a digital computer and Classify and compute the performance of machines, Machine Instructions.
2. Describe various data transfer techniques in digital computer and the I/O interfaces.
3. Analyze the performance of various classes of Memories, build large memories using small memories forbetter performance and analyze arithmetic forALU implementation
4. Describe the basics of hardwired and micro-programmed control of the CPU, pipelined architectures, Hazards and Superscalar Operations

UNIT-1

Section: I (5 Marks)

1. State and explain the two De Morgan Theorems. [Unit 1, CO1, understand] LOT
2. Clarify the duality principle in Boolean Algebra. Show two duals. [Unit 1, CO1, remember] LOT
3. Design the 4-bit parallel binary adder using four full adders using appropriate block digram folloed by a brief description.[Unit 1, CO2, Create] HOT
4. Elucidate SOP and POS Boolean expressions using example(s) for both. [Unit 1, CO1, Analyze] HOT
5. Explain sequential circuit with a proper diagram. [Unit 1, CO2, understand] LOT
6. What do you mean by combinational circuit? Explain it with proper diagram. [Unit 1, CO2, understand] LOT

7. Differentiate between minterms and maxterms giving suitable example.[Unit 1, CO1, understand] LOT
8. State the definition of a register. [Unit 2, CO3, remember] LOT
9. Explain byte addressability. [Unit 2, CO3, understand] LOT
10. Discuss about immediate 32-bit value. [Unit 2, CO1, apply] LOT
11. Differentiate between machine language and assembly language programs. [Unit 2, CO3, remember] LOT
12. Write the difference between opcode and operand. Explain it with an example. [Unit 2, CO3, understand]
13. Draw instruction cycle and explain the various stage of the cycle. [Unit 2, CO1, understand]
14. Differentiate between big endian and little endian with an example. [Unit 2, CO1, evaluate]
15. Illustrate the behavior of a pipeline using space-time diagram. [Unit 3, CO4, understand]
16. List the five levels of parallelism used in a computer. [Unit 3, CO4, remember]
17. Elaborate the terms: a. clock frequency b. Pipeline bubble [Unit 3, CO4, understand]
18. Elaborate the concept of interrupts. How does a processor process interrupts? [Unit 5, CO4, understand]
19. Explain the mathematical derivation of performance gain due to pipeline. [Unit 3, CO4, evaluate]
20. Define the following-: [Unit 3, CO1, understand]
    a. Data bus b. Address bus c. Control bus
21. Compare the two semiconductor RAM memories. [Unit 4, CO3, analyze]
22. Give a comparison of MAR and MDR. [Unit 4, CO3, understand]
23. State the significance of cache memory in the performance of a computer system. [Unit 4, CO3, evaluate]
24. Elaborate the concept of "locality of reference" in cache memory? [Unit 5, CO4, understand]
25. Differentiate between shared memory and distributed memory.[Unit 5, CO4, remember]

Section: II (10 Marks)

26. Prove the following theorems: [Unit 1, CO1, evaluate]
    a) A + A' B = A + B
    b) (A+B) (A+C) = A + BC
27. Prove the following theorems using truth tables: [Unit 1, CO1, evaluate]
    a) A + A' B = A + B
    b) (A+B) (A+C) = A + BC
28. Apply De Morgan's theorems to evaluate the following expressions: [Unit 1, CO1, evaluate]
    a. (X'+Y'+Z')' b. ((W+X)Y)'
29. Define gate. Draw the circuit diagram of full adder using two half adders with appropriate labelling. [Unit 1, CO2, analyze]
30. Draw K map for the Boolean expressing given below and simplify the equation-:
    F(A,B,C,D)= m(1,2, 5, 7, 8, 9, 11, 12, 14) [Unit 1, CO2, evaluate]

31. Convert the following Boolean expression into standard SOP/POS form. [Unit 1, CO1, evaluate]
    a. AB + AC' + BC'
    b. (A + B' + C') (A+B'+C'+D) (B'+C+D)
32. Define multiplexer. Draw 4 is to 1 multiplexer with logic diagram and truth table. [Unit 1, CO2, apply]
33. Draw the Karnaugh map of the following SOP expression: [Unit 1, CO2, Apply]
    A'B'C'D'+A'BC'D'+A'BCD+ABC'D+AB'C'D'+AB'CD
34. Draw and explain the design of half adder and full adder circuit using logic gates. [Unit 1, CO2, analyze]
35. State the significance of addressing mode. Compare immediate and direct addressing modes. [Unit 2, CO3, analyze]
36. Evaluate the terms (with example): a. memory word b. Subroutines [Unit 2, CO3, evaluate]
37. Explain the four stage of instruction pipelining of four instructions. [Unit 3, CO4, evaluate]
38. Give an analytical approach of the CISC style processor in detail. [Unit 3, CO4, analyze]
39. Give a technical view of the Hardwired control unit in detail. [Unit 3, CO4, analyze]
40. A non-pipeline system takes 50ηs to process a task. The same task can be processed in a six – segment pipeline with a clock of 10 ηs. Determine speedup ratio of the pipeline for 100 tasks. [Unit 3, CO4, evaluate]
41. Give an overview of the types of cache memory. [Unit 4, CO3, analyze]

Section: III (20 Marks)

43. a.State the difference between decoder and encoder circuits. Design the logic circuit diagram of 3 to 8 line decoder and the corresponding truth table. [Unit 1, CO2, Analyze & Evaluate]
    b. Draw the block digram, truth table and logic circit diagram of Decimal to BCD encoder circuit. [Unit 1, CO2, Analyze & Evaluate]
44. Illustrate the concept of flip flop. Draw the logic diagram and write the characteristic table of any two the following flip flops-: [Unit 1, CO2, evaluate]
    a. RS flip flop
    b. JK flip flop
    c. D flip flop
45. Provide an analytical view of five commonly used memory addressing modes. [Unit 2, CO3, analyze]
46. Explain pipeline hazard. Describe the issue of data dependency and illustrate data dependency for a six stage pipeline for the following two successive instructions.
    Add R1, R2
    Sub R1, R2 [Unit 3, CO4, evaluate]
47. Explain the varius types of data dependency hazard. Give suitable example for each.[Unit 3, CO4, analyze & evaluate]
48. Discuss the Flynn's classification of processors in the features of different levels in detail. [Unit 5, CO4, Analyse]

49. Illustrate the significance of virtual memory in a system. Discuss the process of virtual memory management? [Unit 4, CO3, Evaluate]
50. Analyze the cache coherence issue. Explain the various solutions that are implemented to overcome this issue. [Unit 5, CO4, Analyze]

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Disclaimer: - This is a Practice Set. The Question in End term examination will differ from the Practice set. This Practice set is meant for practice only.